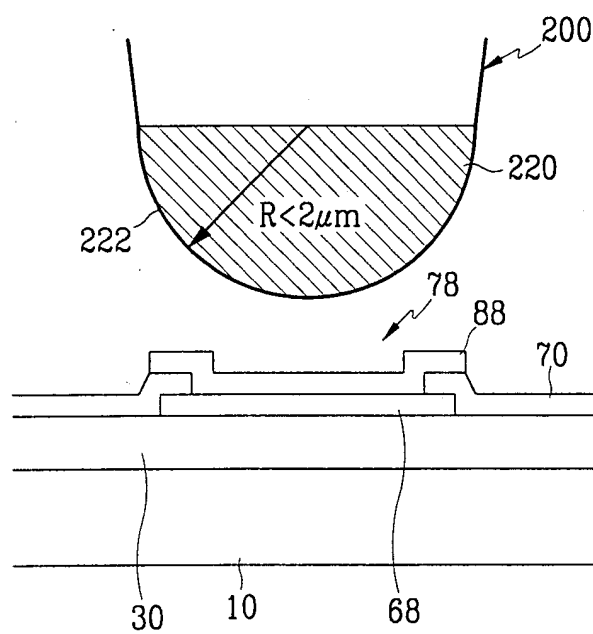


A cross-sectional view of a semiconductor device. A curved layer 200 is shown above a structure 70. A shaded region 220 within the curved layer 200 has a radius $R < 2\mu\text{m}$. The structure 70 includes features 78 and 88. The device is built on a substrate 10, which includes layers 30 and 68.



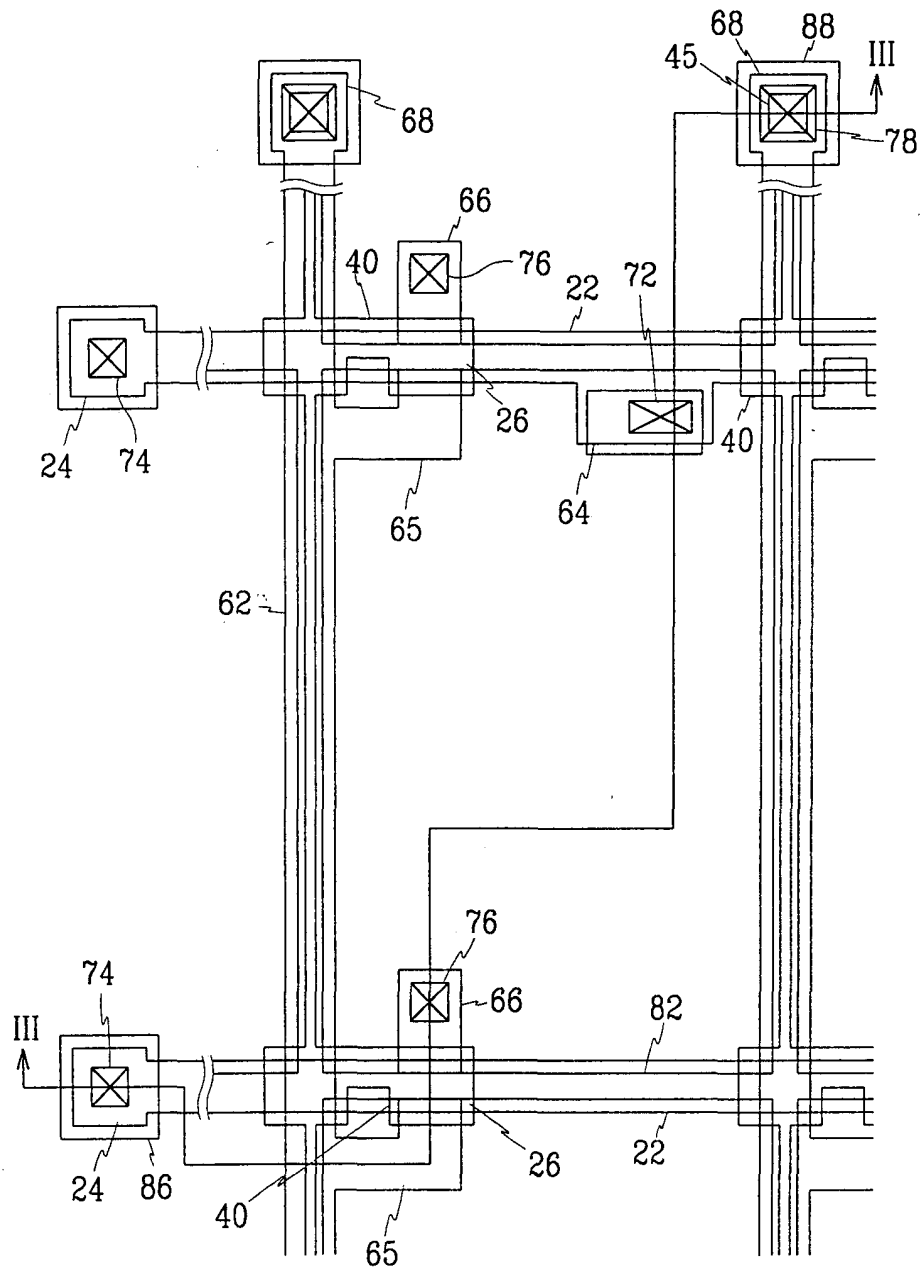


FIG. 4

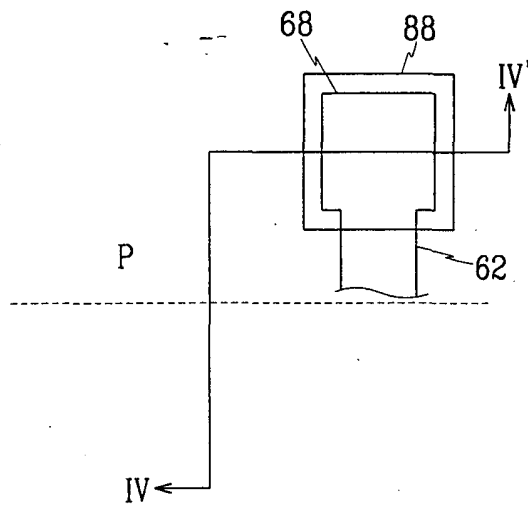


FIG. 5

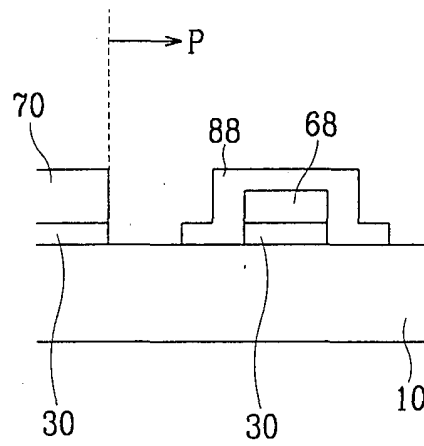


FIG. 6

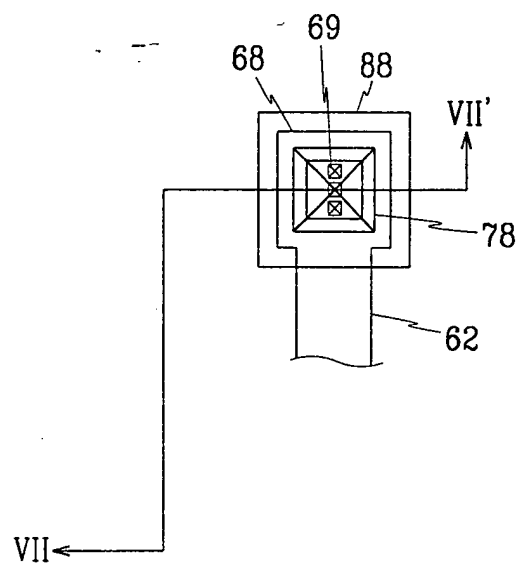


FIG. 7

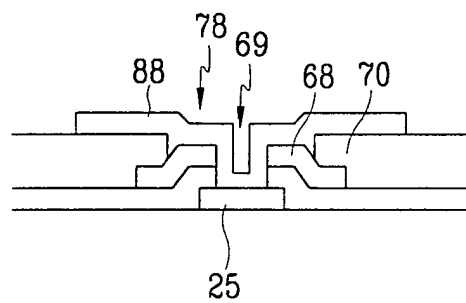


FIG. 8A

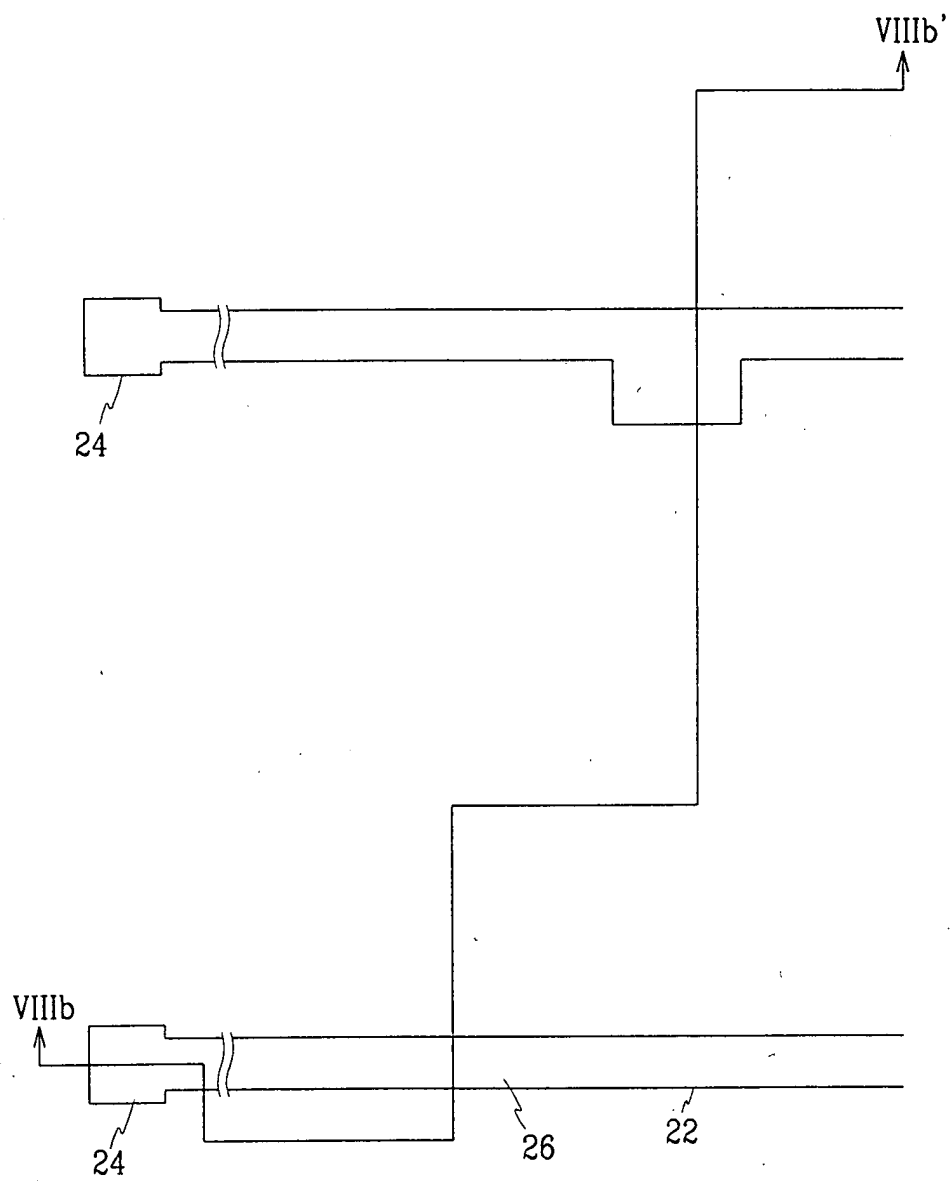


FIG. 8B

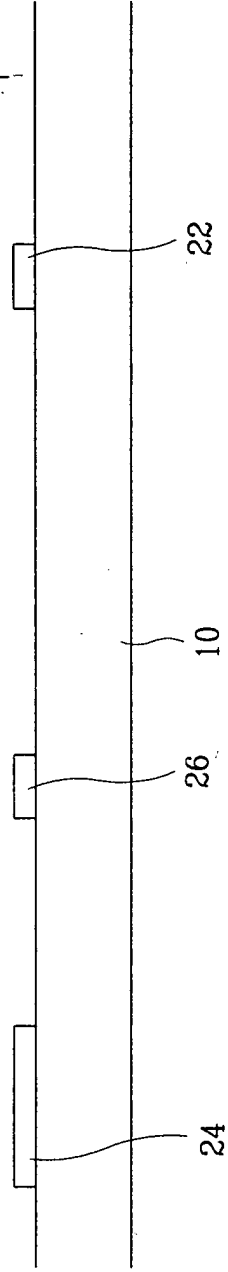


FIG. 9A

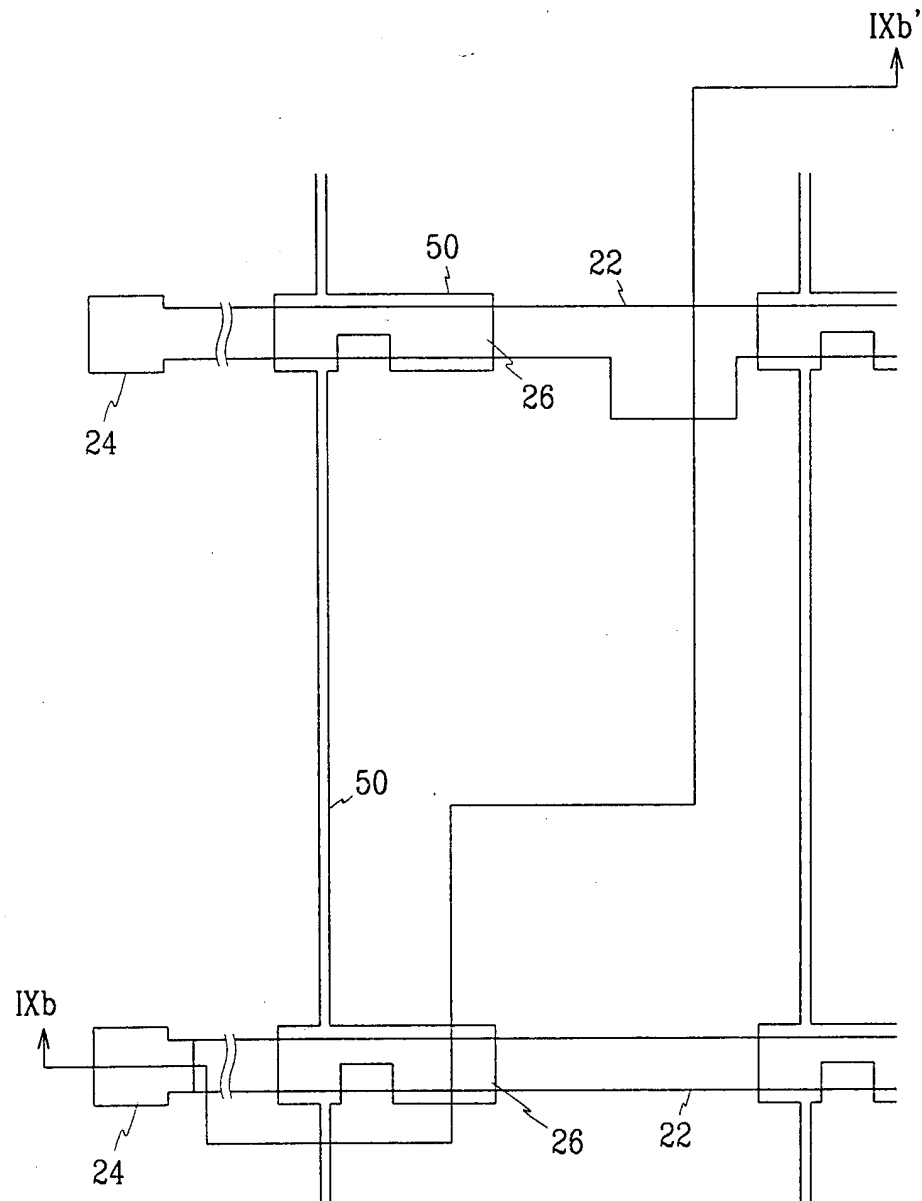


FIG. 9B

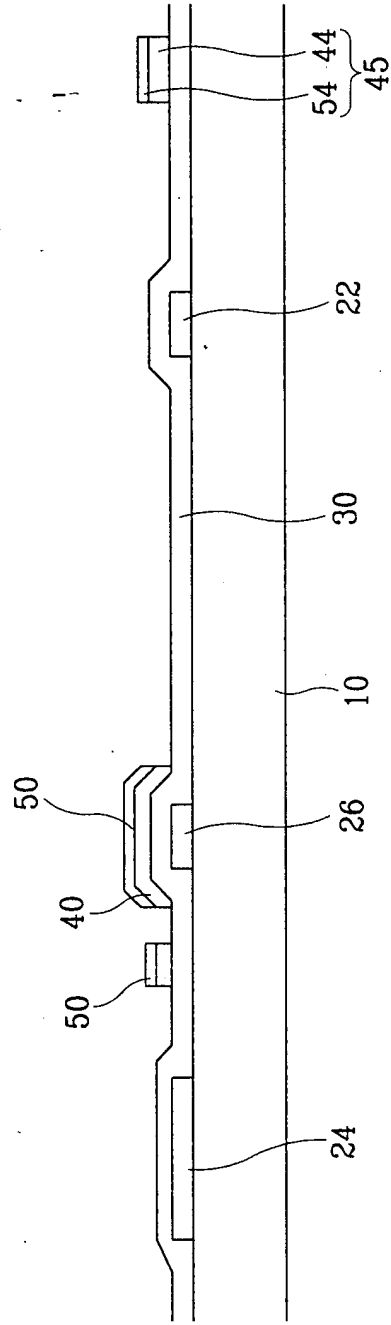


FIG. 10A

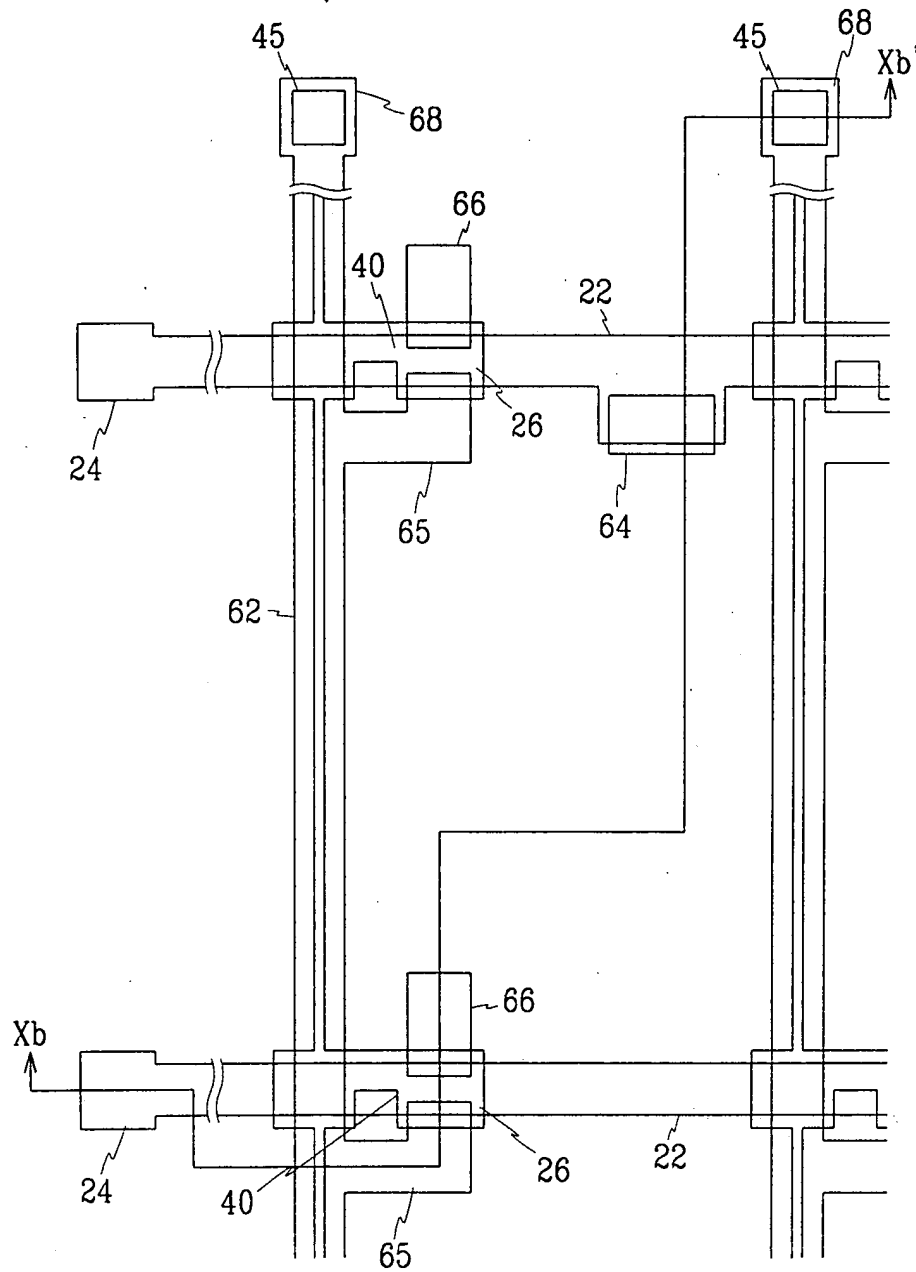


FIG. 10B

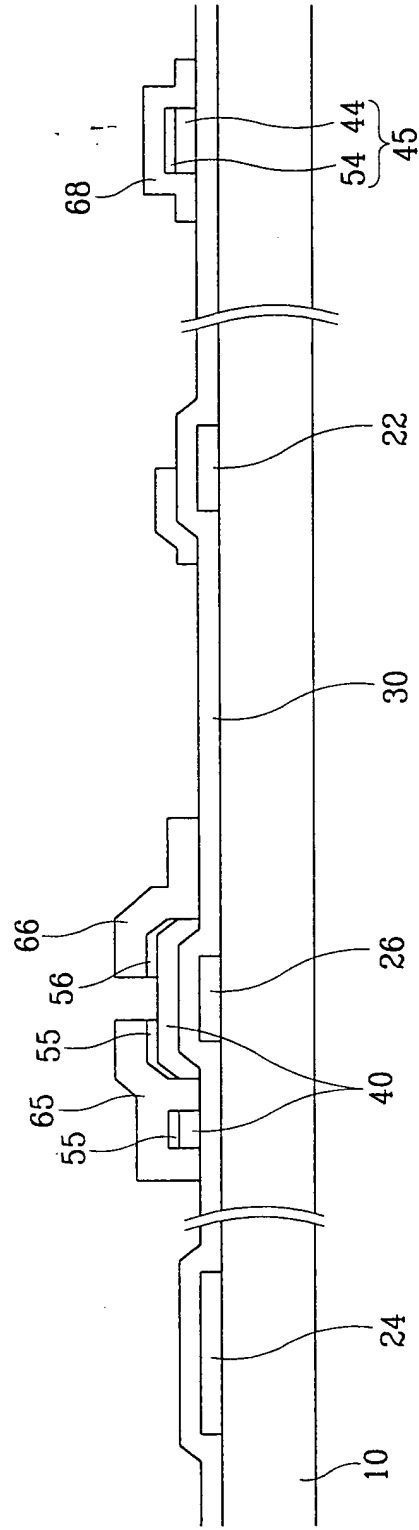


FIG. 11A

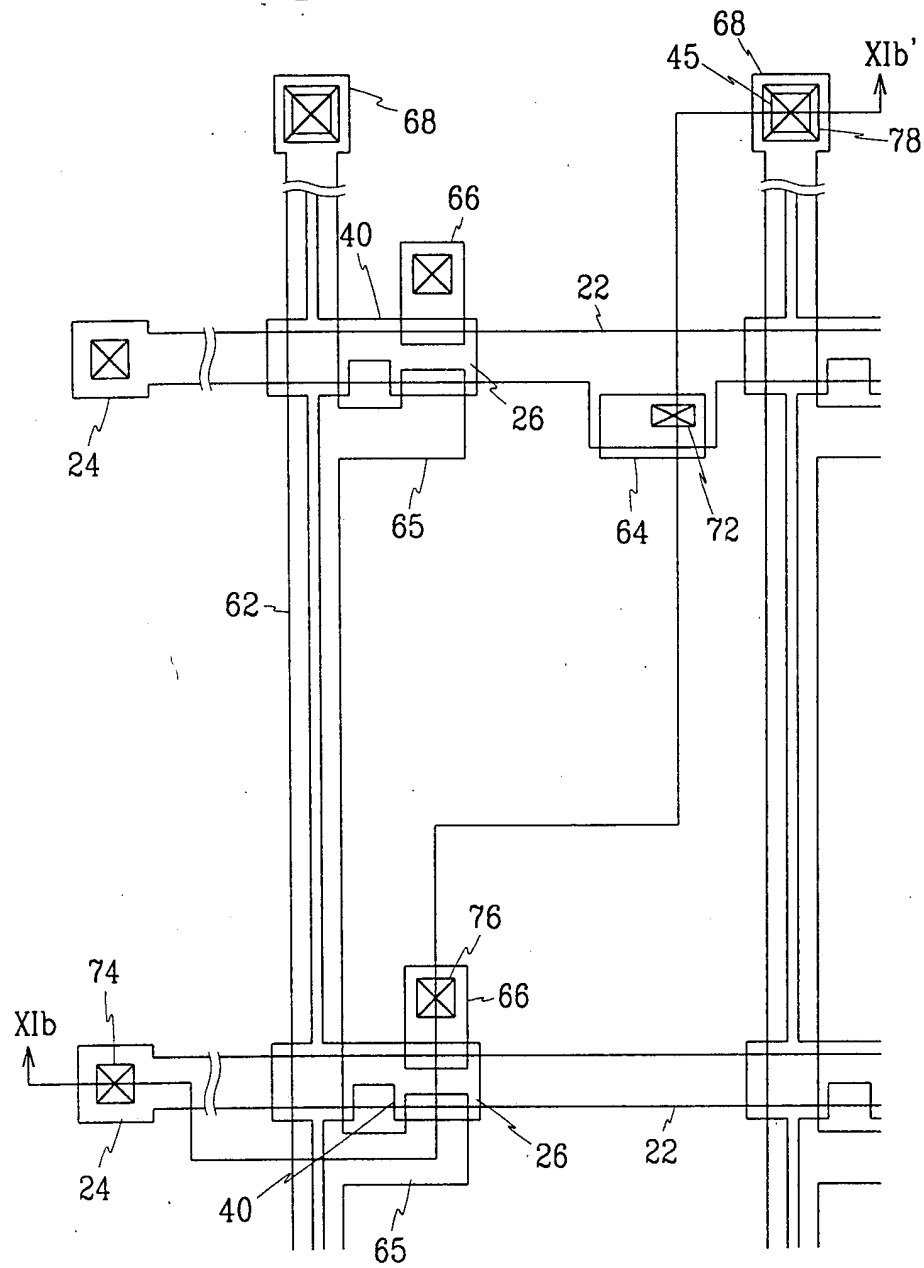


FIG. 12

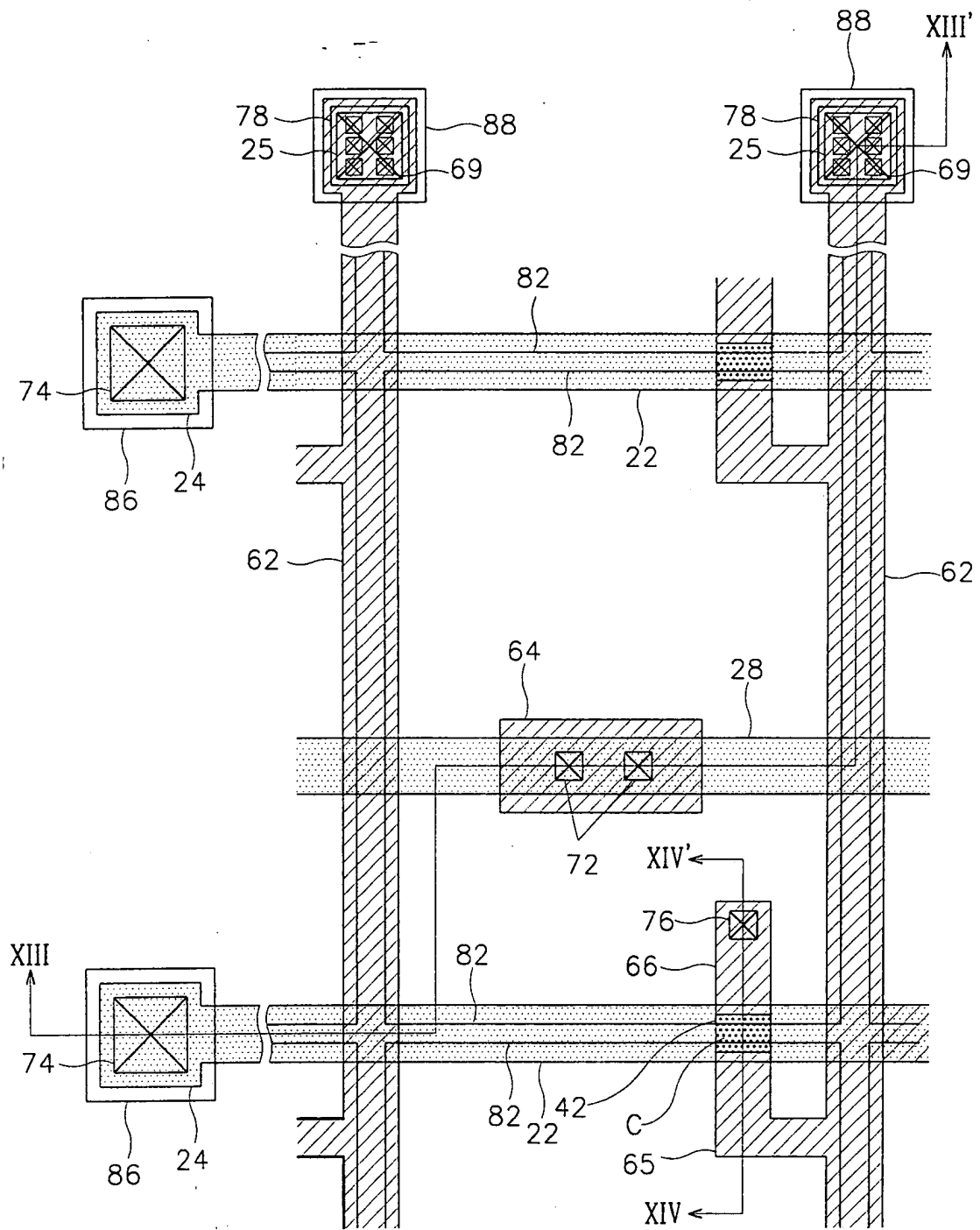


FIG. 13

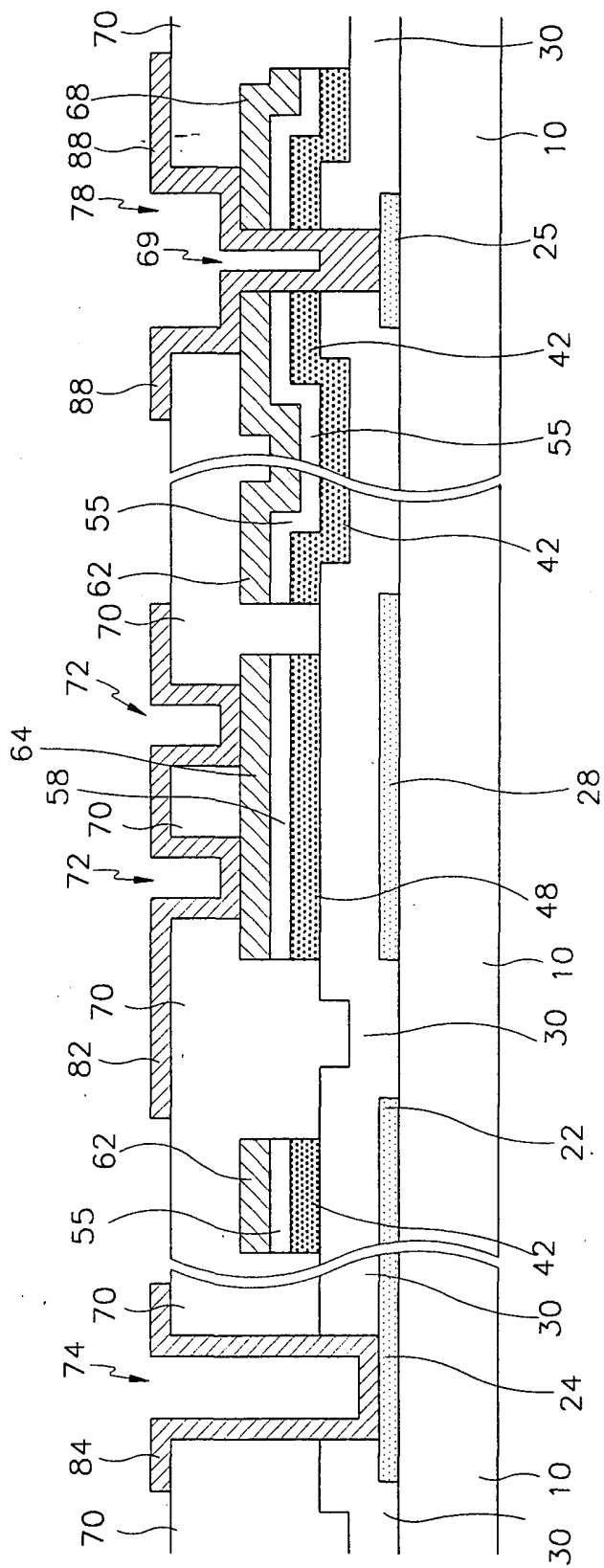


FIG. 15A

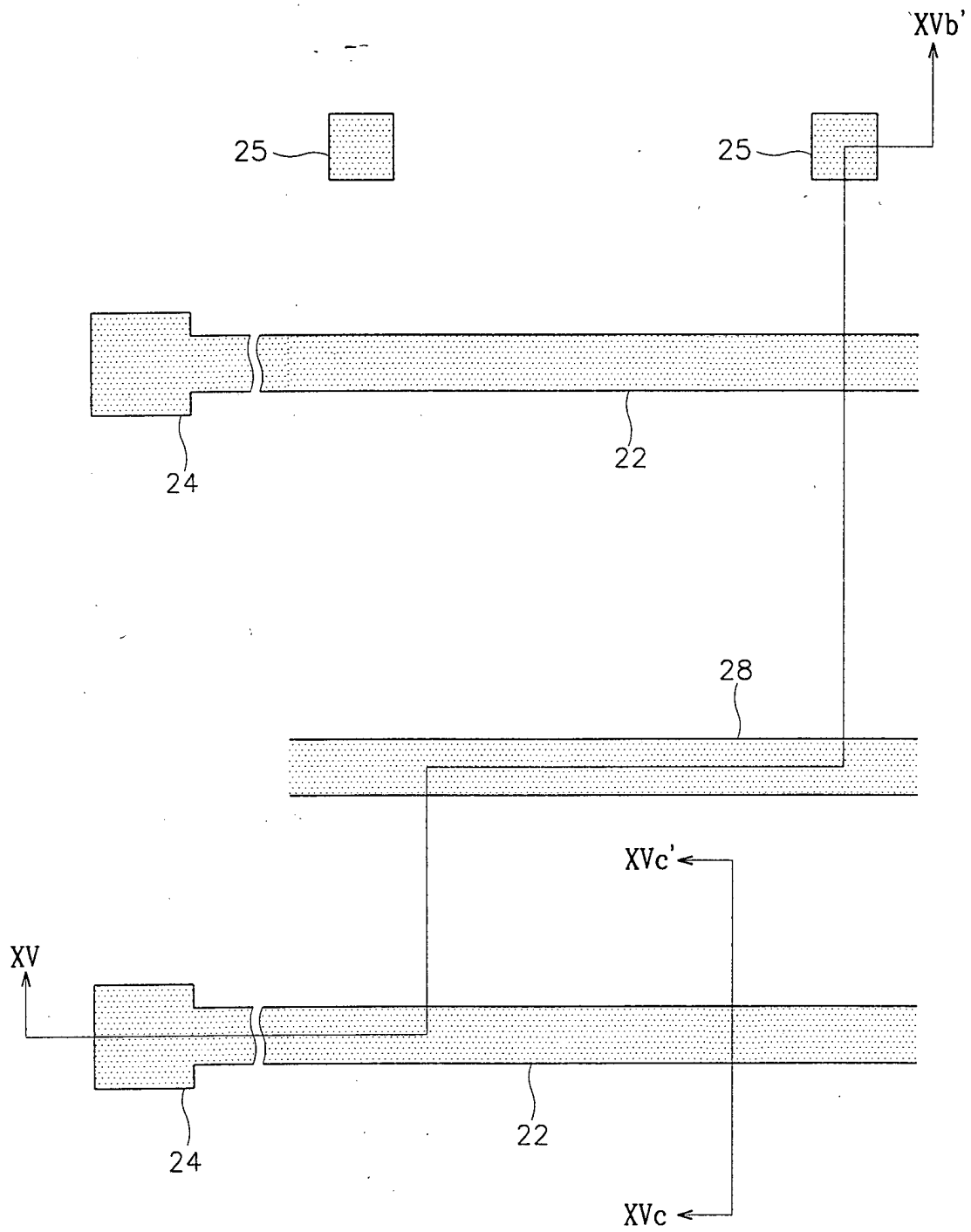


FIG. 15B

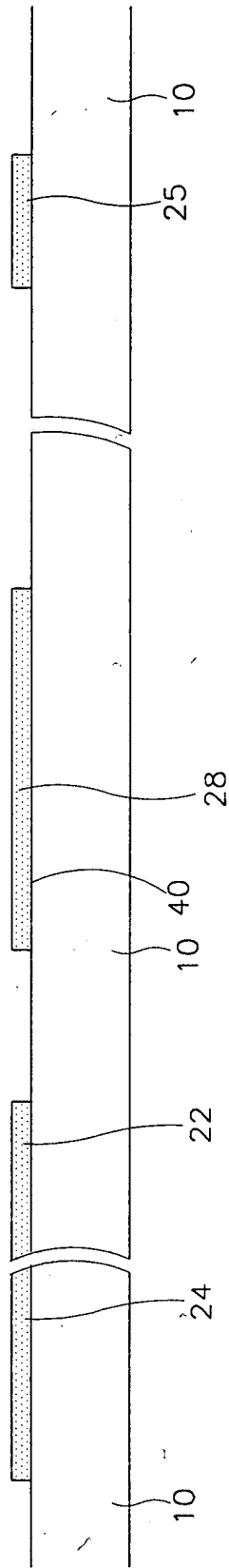


FIG. 15C

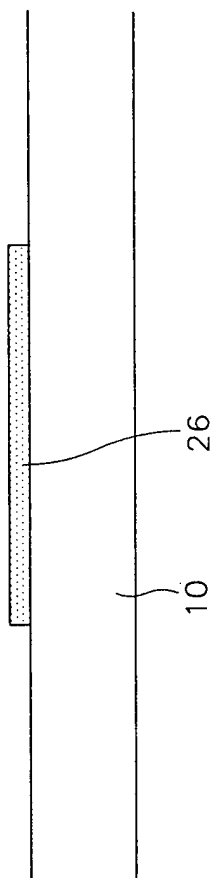


FIG. 16B

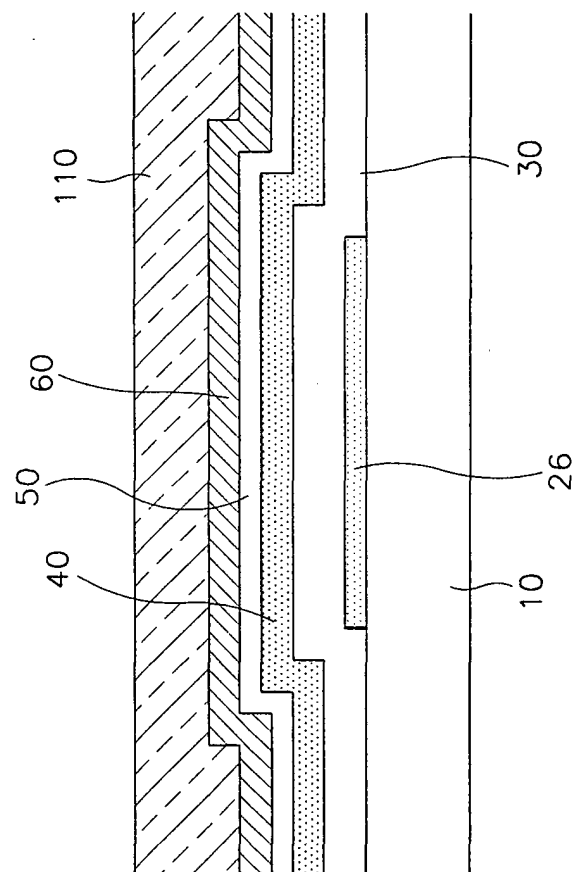


FIG. 17A

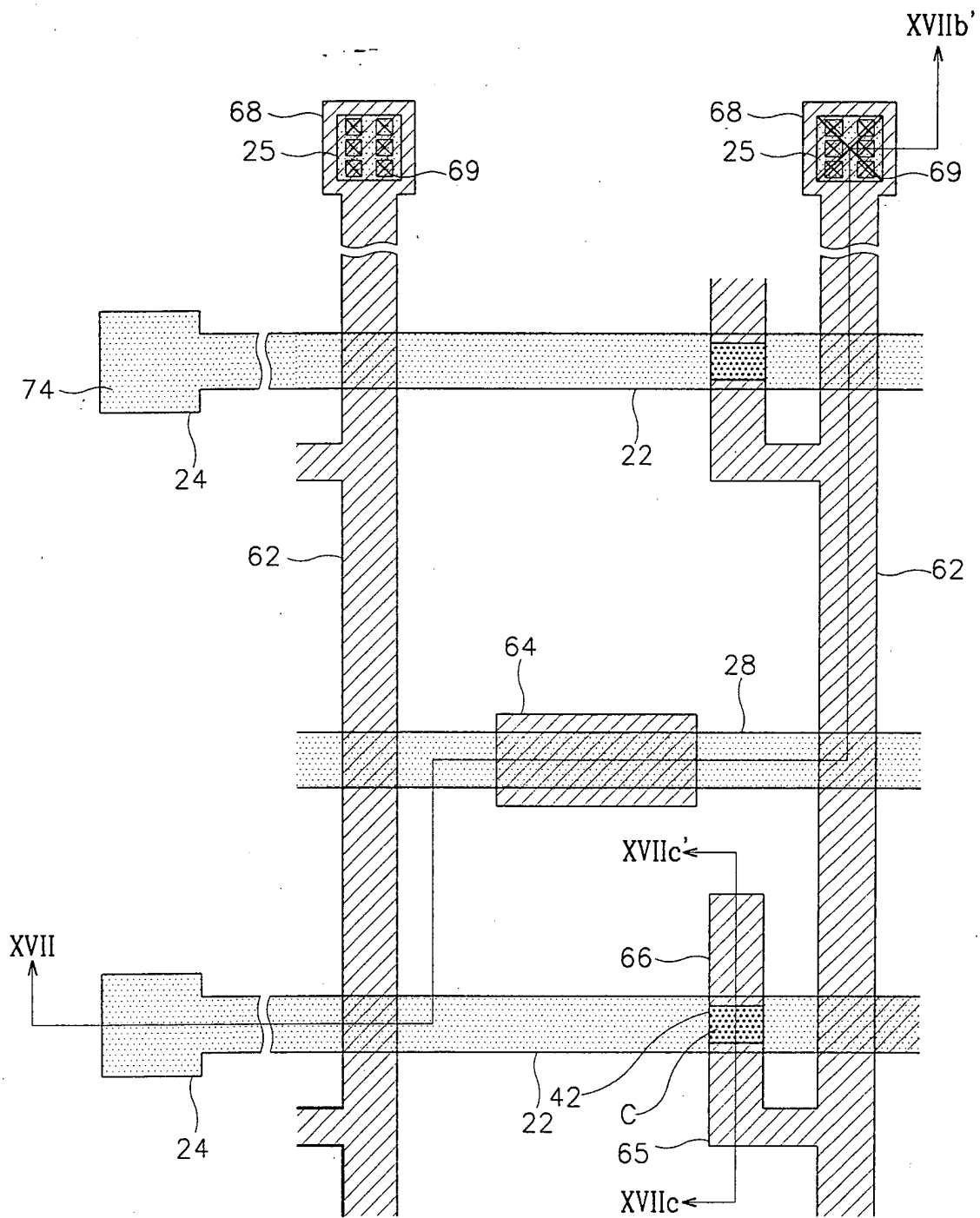


FIG. 17C

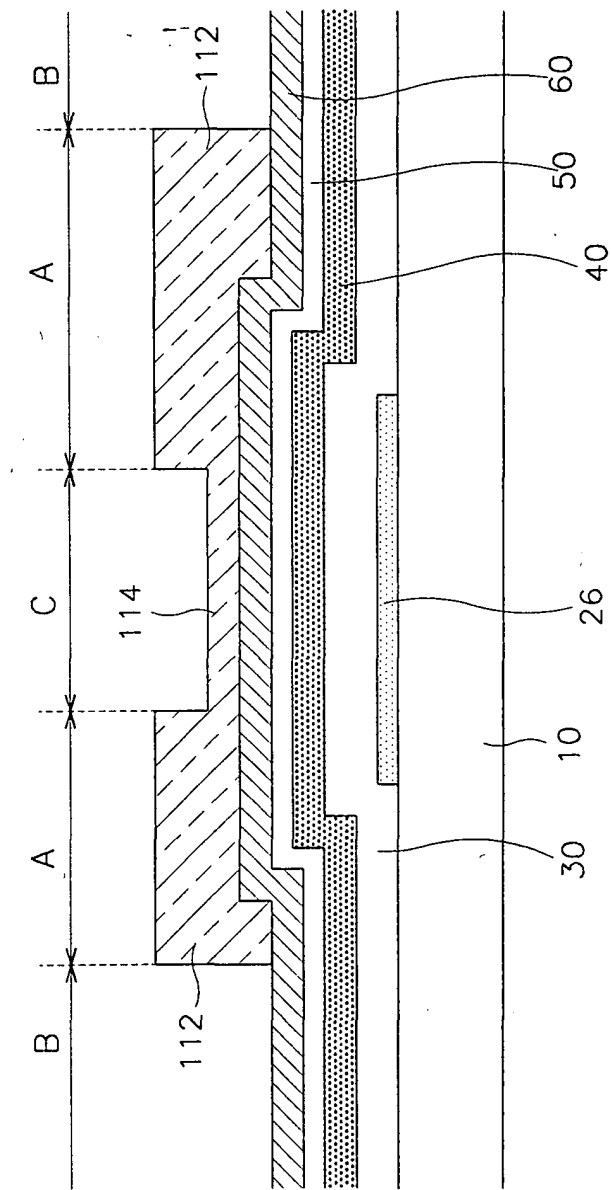
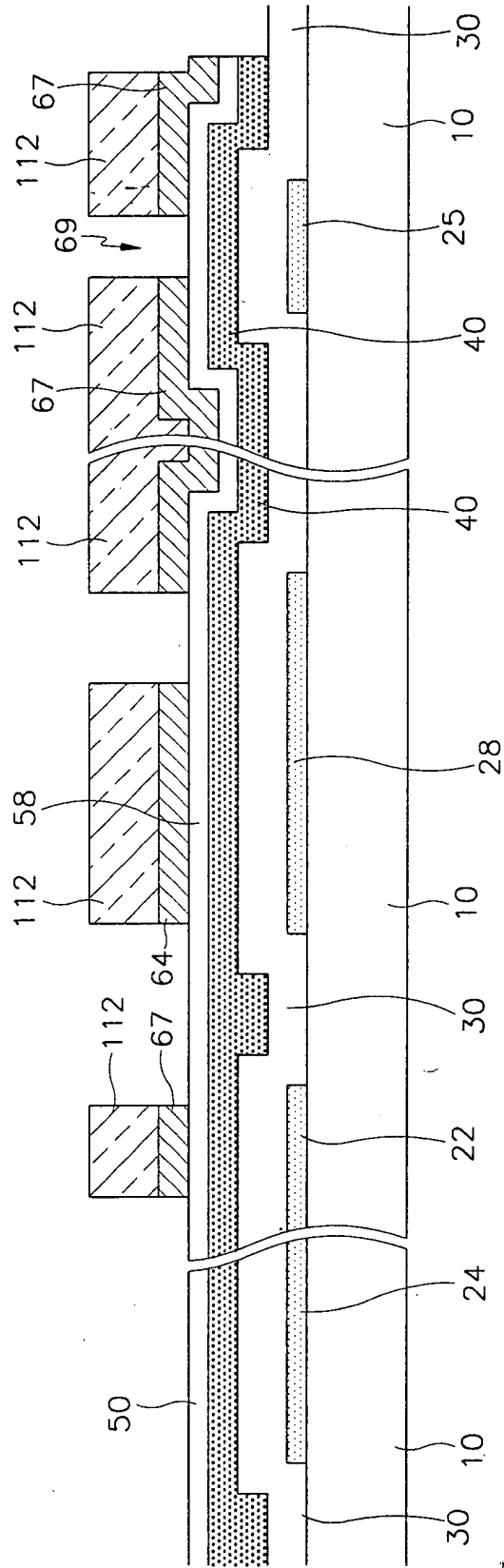
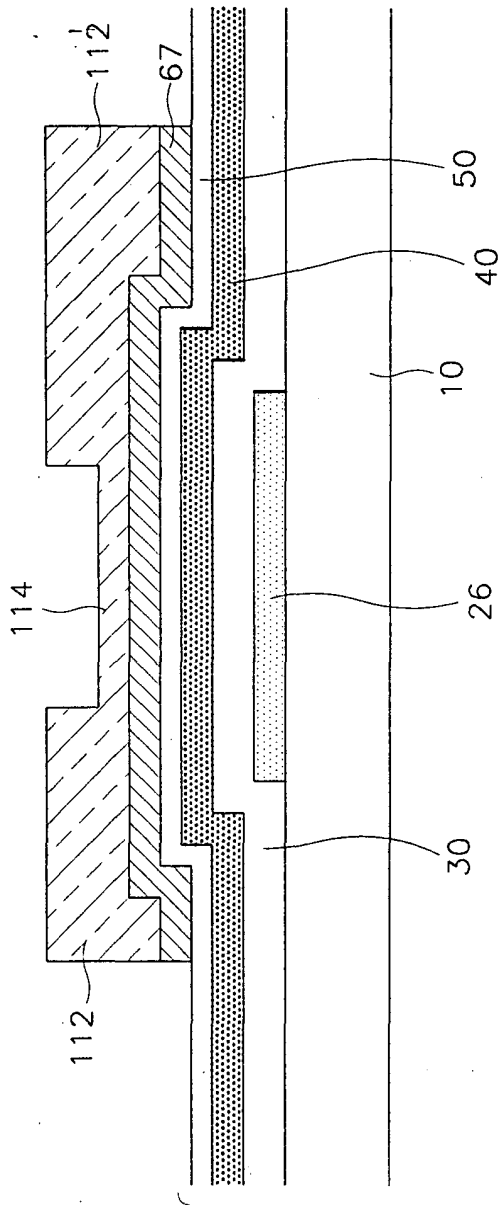


FIG. 18A





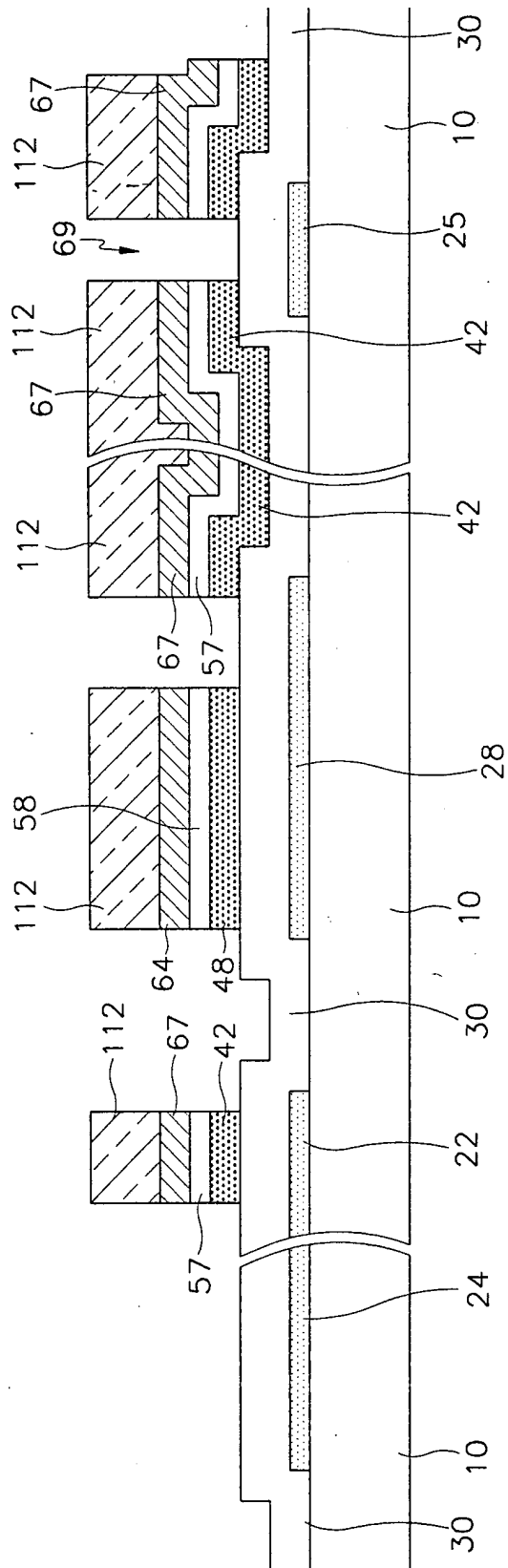


FIG. 19B

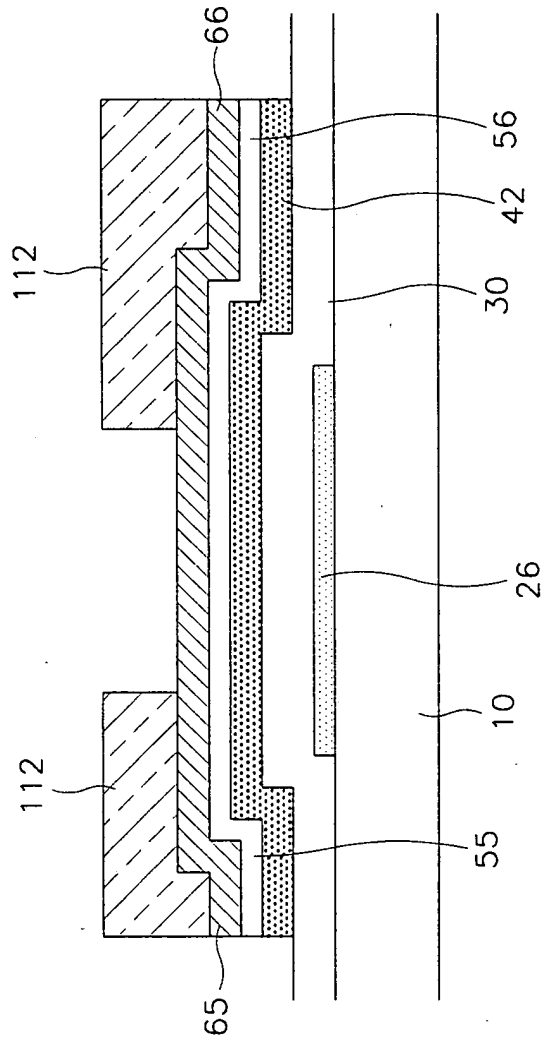


FIG. 20B

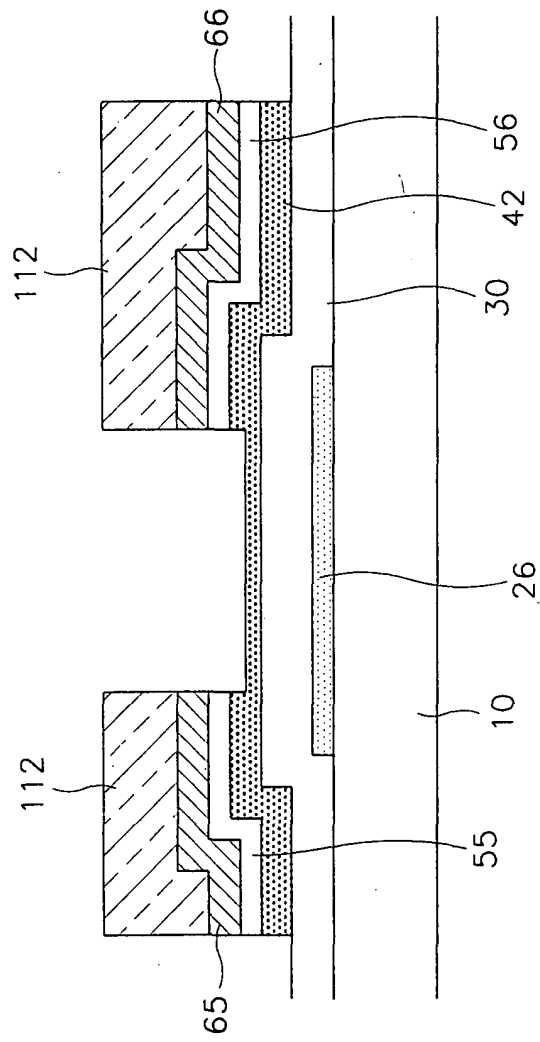


FIG. 21A

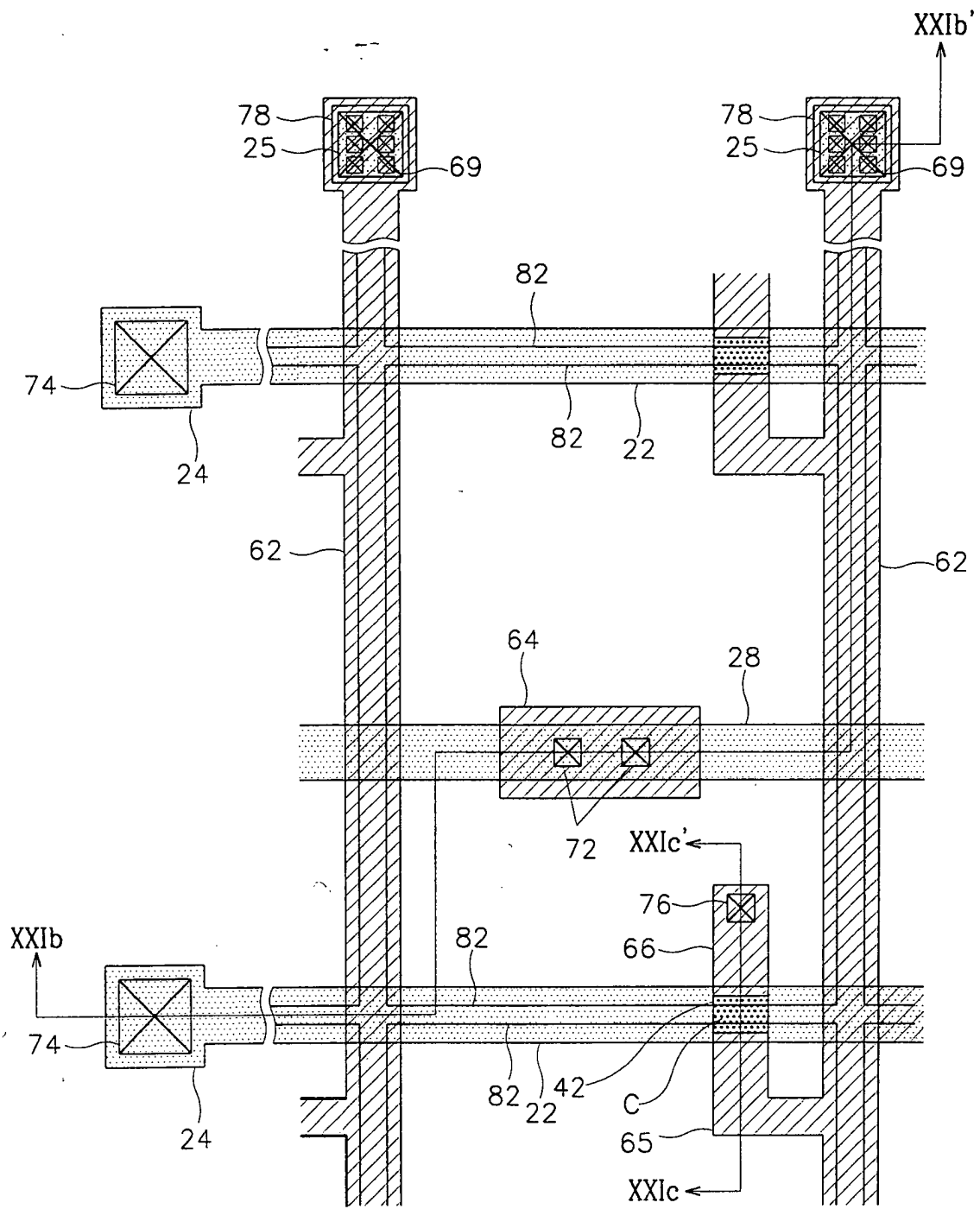
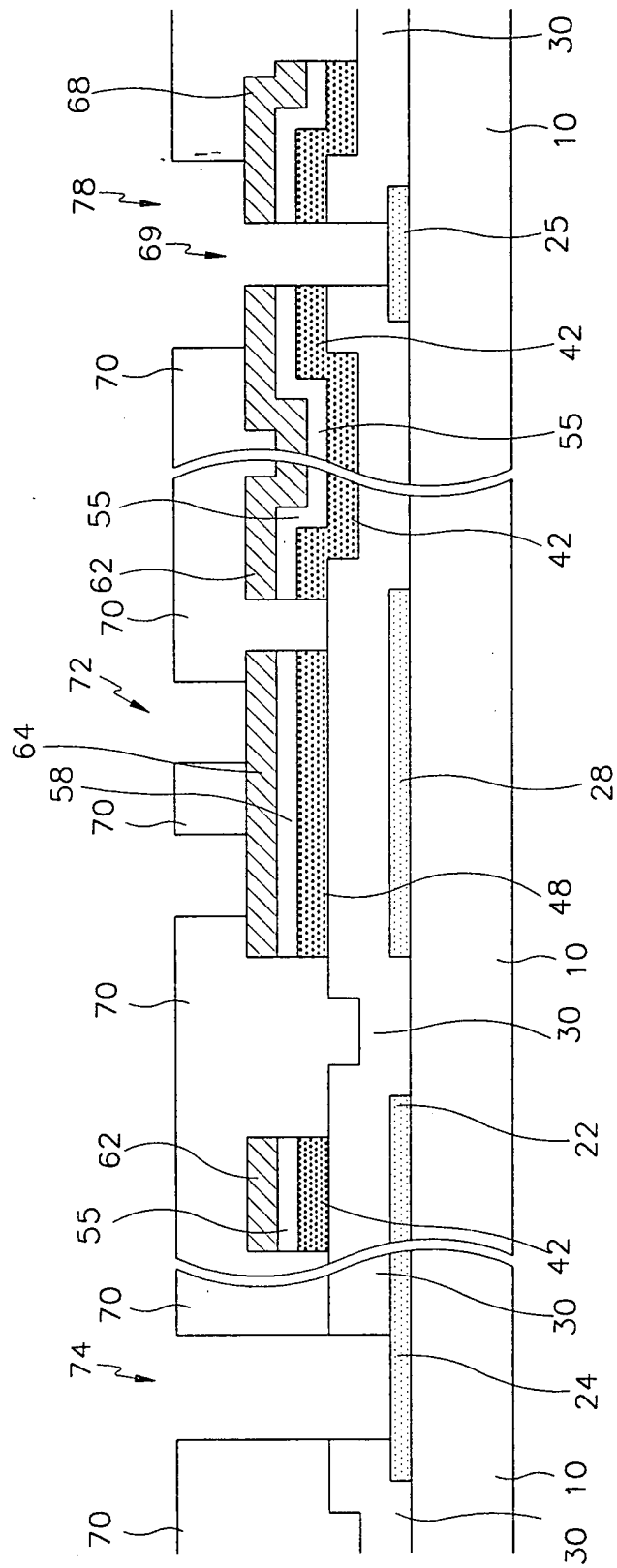


FIG. 21B



This cross-sectional view shows a central channel region (30) flanked by side gate regions (55, 65). The channel is defined by a central layer (26) and is surrounded by a gate stack (42). The side gates are formed by a stack of layers (56, 66) on top of the channel. The device is situated on a substrate (70) with a top surface (76). The channel region (30) is shown with a dotted pattern, while the side gate regions (55, 65) are shown with a hatched pattern. The gate stack (42) is shown with a solid pattern. The substrate (70) is shown with a solid pattern. The top surface (76) is indicated by an arrow.

FIG. 22

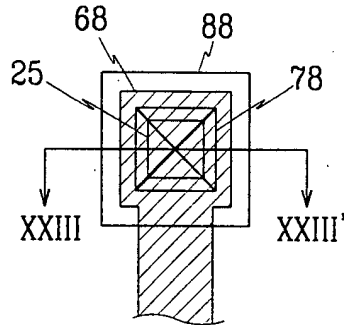


FIG. 23

